CLAIMS

What is claimed is:

1	1.	A protective structure for blocking the propagation of defects generated in		
2	a semiconduc	a semiconductor device, the structure comprising:		
3		a deep trench isolation formed between a memory storage region of the		
4	semiconducto	or device and a logic circuit region of the semiconductor device, said deep		
5	trench isolati	trench isolation being filled with an insulative material;		
6		wherein said deep trench isolation prevents the propagation of crystal		
7	defects generated in said logic circuit region from propagating into said memory storage			
8	region.			
1	2.	The structure of claim 1, wherein said deep trench isolation is formed		
2	beneath a sha	beneath a shallow trench isolation, said shallow trench isolation for electrically isolating		
3	devices conta	devices contained in said memory storage region from devices contained in said logic		
4	circuit region	circuit region.		
1	3.	The structure of claim 1, further comprising a plurality of deep trench		
2		rounding said memory storage region.		
2	isolations sai	rounding said momory storage region.		
1	4.	The structure of claim 3, wherein said plurality of deep trench isolations		
2	further comp	further comprise:		
3		an inner perimeter and an outer perimeter, wherein individual deep trench		
4	isolations included in said outer perimeter are disposed adjacent to gaps in between			

individual deep trench isolations included in said inner perimeter.

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1	5.	The structure of claim 1, wherein said memory storage region comprises a	
2	DRAM array	y region.	
1	6	The structure of claims 5 whomain gold DD AM arrow region includes a	
1	6.	The structure of claim 5, wherein said DRAM array region includes a	
2	plurality of o	deep trench storage capacitors.	
1	7.	The structure of claim 6, wherein said logic circuit region further includes:	
2		a plurality of CMOS devices; and	
3		a high dose impurity layer implanted within a substrate of said logic circuit	
4	region, said	region, said high dose impurity layer used to inhibit parasitic bipolar transistor action	
5	between said	d plurality of CMOS devices.	
1	8.	An embedded DRAM (eDRAM) device, comprising:	
2		a logic circuit region;	
3		a memory storage region embedded within said logic circuit region;	
4		a shallow trench isolation for electrically insulating devices included	
5	within said	within said memory storage region from devices included within said logic circuit region	
6	and		
7		a deep trench isolation, formed underneath said shallow trench isolation,	
8	said deep tre	said deep trench isolation for preventing the propagation of crystal defects generated in	
9	said logic ci	said logic circuit region from propagating into said memory storage region.	
1	9.	The eDRAM device of claim 8, wherein said shallow trench isolation	
2	surrounds sa	surrounds said memory storage region.	

1	10.	The eDRAM device of claim 9, further comprising a plurality of deep		
2	trench isolati	trench isolations surrounding said memory storage region.		
1	11.	The eDRAM device of claim 10, wherein said plurality of deep trench		
2	isolations further comprise:			
3		an inner perimeter and an outer perimeter, wherein individual deep trench		
4	isolations included in said outer perimeter are disposed adjacent to gaps in between			
5	individual de	individual deep trench isolations included in said inner perimeter.		
1	12.	The eDRAM device of claim 11, wherein said memory storage region		
2	includes a pl	lurality of deep trench storage capacitors.		
1	13.	The eDRAM device of claim 12, wherein said logic circuit region further		
2	includes:			
3		a plurality of CMOS devices; and		
4		a high dose impurity layer implanted within a substrate of said logic circuit		
5	region, said	region, said high dose impurity layer used to inhibit parasitic bipolar transistor action		
6	between said	between said plurality of CMOS devices.		

1	14.	A method for blocking the propagation of defects generated in a		
2	semiconductor device, the method comprising:			
3		forming a deep trench isolation formed between a memory storage region		
4	of the semico	onductor device and a logic circuit region of the semiconductor device; said		
5	deep trench i	deep trench isolation being filled with an insulative material;		
6		wherein said deep trench isolation prevents the propagation of crystal		
7	defects gener	defects generated in said logic circuit region from propagating into said memory storage		
8	region.			
1	15.	The method of claim 14, wherein said deep trench isolation is formed		
2	beneath a shallow trench isolation, said shallow trench isolation for electrically isolating			
3	devices conta	devices contained in said memory storage region from devices contained in said logic		
4	circuit region	l.		
1	16.	The method of claim 14, further comprising forming a plurality of deep		
2	trench isolati	trench isolations to surround said memory storage region.		
1	17.	The method of claim 16, further comprising:		
2		configuring said deep trench isolations to form an inner perimeter and an		
3	outer perimet	outer perimeter, wherein individual deep trench isolations included in said outer		
4	perimeter are	perimeter are disposed adjacent to gaps in between individual deep trench isolations		
5	included in sa	included in said inner perimeter.		
1	18.	The method of claim 14, wherein said memory storage region comprises a		
2	DRAM array region.			

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1	19.	The method of claim 18, wherein said DRAM array region includes a	
2	plurality of deep trench storage capacitors.		
1	20.	The method of claim 19, wherein said logic circuit region further includes:	
2		a plurality of CMOS devices; and	
3		a high dose impurity layer implanted within a substrate of said logic circuit	
4	region, said h	region, said high dose impurity layer used to inhibit parasitic bipolar transistor action	
5	between said plurality of CMOS devices.		